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| L2 | 661 | 714/748.ccls. | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/13 18:59 |
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| L4 | 1949 | 341/143.ccls. | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/13 19:04 |
| L5 | 6240 | sigma adj5 delta | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2006/06/13 19:06 |
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IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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- ☐ 1. **Coding, decoding, and recovery of clock synchronization in digital multiplexers**
 Hansheng Wang; Xiaoyi Qin; Lieguang Zeng; Fuqin Xiong;
Communications, IEEE Transactions on
 Volume 51, Issue 5, May 2003 Page(s):825 - 831
 Digital Object Identifier 10.1109/TCOMM.2003.811432
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(456 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ 2. **A multiband /spl Delta//spl Sigma/ fractional-N frequency synthesizer for transceiver RFIC**
 Rogers, J.W.M.; Dai, F.F.; Cavin, M.S.; Rahn, D.G.;
Solid-State Circuits, IEEE Journal of
 Volume 40, Issue 3, Mar 2005 Page(s):678 - 689
 Digital Object Identifier 10.1109/JSSC.2005.843604
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(1552 KB\)](#) IEEE JNL
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IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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- ☐ **1. Two-stage sigma-delta modulation**
 Wong, P.W.; Gray, R.M.;
[Acoustics, Speech, and Signal Processing \[see also IEEE Transactions on Sig IEEE Transactions on](#)
 Volume 38, Issue 11, Nov. 1990 Page(s):1937 - 1952
 Digital Object Identifier 10.1109/29.103095
[AbstractPlus](#) | Full Text: [PDF\(1028 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **2. A digital fluxgate magnetic sensor interface using sigma-delta modulation magnetic field measurement**
 Kawahito, S.; Cerman, A.; Tadokoro, Y.;
[Instrumentation and Measurement Technology Conference, 2002. IMTC/2002. the 19th IEEE](#)
 Volume 1, 21-23 May 2002 Page(s):257 - 260 vol.1
 Digital Object Identifier 10.1109/IMTC.2002.1006849
[AbstractPlus](#) | Full Text: [PDF\(443 KB\)](#) IEEE CNF
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- ☐ **3. Multi-loop sigma-delta quantization: spectral analysis**
 He, N.; Buzo, A.; Kuhlmann, F.;
[Acoustics, Speech, and Signal Processing, 1988. ICASSP-88., 1988 Internatio on](#)
 11-14 April 1988 Page(s):1870 - 1873 vol.3
 Digital Object Identifier 10.1109/ICASSP.1988.196989
[AbstractPlus](#) | Full Text: [PDF\(236 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ **4. Mismatch shaping for a current-mode multibit delta-sigma DAC**
 Tao Shui; Schreier, R.; Hudson, F.;
[Solid-State Circuits, IEEE Journal of](#)
 Volume 34, Issue 3, March 1999 Page(s):331 - 338
 Digital Object Identifier 10.1109/4.748184
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(348 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **5. A CMOS 0.8- μ m transistor-only 1.63-MHz switched-current bandpass $\Sigma\Delta$ AM signal A/D conversion**
 de la Rosa, J.M.; Perez-Verdu, B.; del Rio, R.; Rodriguez-Vazquez, A.;
[Solid-State Circuits, IEEE Journal of](#)
 Volume 35, Issue 8, Aug. 2000 Page(s):1220 - 1226
 Digital Object Identifier 10.1109/4.859514

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(204 KB\)](#) IEEE JNL
[Rights and Permissions](#)

- ☐ **6. Post modulator filtering in /spl Delta/-/spl Sigma/ fractional-N frequency s**
Borkowski, M.J.; Kostamovaara, J.;
[Circuits and Systems, 2004. MWSCAS '04. The 2004 47th Midwest Symposium on](#)
Volume 1, 25-28 July 2004 Page(s):1 - 325-8 vol.1
Digital Object Identifier 10.1109/MWSCAS.2004.1353993
[AbstractPlus](#) | Full Text: [PDF\(481 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ **7. A 3.3 V switched-current second order sigma-delta modulator for audio a**
Loulou, M.; Dallet, D.; Marchegay, P.;
[Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE Symposium on](#)
Volume 4, 28-31 May 2000 Page(s):409 - 412 vol.4
Digital Object Identifier 10.1109/ISCAS.2000.858775
[AbstractPlus](#) | Full Text: [PDF\(288 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ **8. New stability criteria for the design of low-pass sigma-delta modulators**
van Engelen, J.A.E.P.; van de Plassche, J.;
[Low Power Electronics and Design, 1997. Proceedings., 1997 International Symposium on](#)
18-20 Aug 1997 Page(s):114 - 118
[AbstractPlus](#) | Full Text: [PDF\(360 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ **9. Efficient narrowband FIR and IFIR filters based on powers-of-two sigma-delta truncation**
Powell, S.R.; Chau, P.M.;
[Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on](#)
[Circuits and Systems II: Express Briefs, IEEE Transactions on](#)
Volume 41, Issue 8, Aug. 1994 Page(s):497 - 505
Digital Object Identifier 10.1109/82.318938
[AbstractPlus](#) | Full Text: [PDF\(752 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **10. Design and high-speed testing of a superconducting delta-sigma oversa**
Xiao, P.H.; Hebert, D.; Whiteley, S.R.; Van Duzer, T.;
[Applied Superconductivity, IEEE Transactions on](#)
Volume 5, Issue 2, Part 3, Jun 1995 Page(s):2264 - 2267
Digital Object Identifier 10.1109/77.403036
[AbstractPlus](#) | Full Text: [PDF\(308 KB\)](#) IEEE JNL
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- ☐ **11. Halftone to continuous-tone conversion of error-diffusion coded images**
Hein, S.; Zakhor, A.;
[Image Processing, IEEE Transactions on](#)
Volume 4, Issue 2, Feb. 1995 Page(s):208 - 216
Digital Object Identifier 10.1109/83.342186
[AbstractPlus](#) | Full Text: [PDF\(1128 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **12. Lowpass double-sampling switched-current sigma-delta modulator**
Garcia, M.A.; Espinosa, G.; Lopez, D.B.;
[Circuits and Systems, 1999. 42nd Midwest Symposium on](#)
Volume 1, 8-11 Aug. 1999 Page(s):47 - 50 vol. 1
Digital Object Identifier 10.1109/MWSCAS.1999.867206
[AbstractPlus](#) | Full Text: [PDF\(292 KB\)](#) IEEE CNF
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- ☐ **13. Higher order sigma-delta modulation encoding for the design of efficient**

FIR filters with powers-of-two coefficients

Chao-Liang Chen; Wilson, A.N., Jr.;

[Circuits and Systems, 1997. ISCAS '97., Proceedings of 1997 IEEE International](#)

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Digital Object Identifier 10.1109/ISCAS.1997.612797

[AbstractPlus](#) | Full Text: [PDF](#)(380 KB) [IEEE CNF](#)[Rights and Permissions](#)**14. Realization of the LMS algorithm with $\Sigma\Delta$ input signals**

Pfann, E.; Stewart, R.W.;

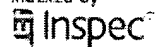
[Signals, Systems and Computers, 1996. 1996 Conference Record of the Thirtieth Conference on](#)

Volume 1, 3-6 Nov. 1996 Page(s):420 - 424 vol.1

Digital Object Identifier 10.1109/ACSSC.1996.600939

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1 [New stability criteria for the design of low-pass sigma-delta modulators](#)



J. A. E. P. van Engelen, R. J. van de Plassche

 August 1997 **Proceedings of the 1997 international symposium on Low power electronics and design**

Publisher: ACM Press

 Full text available: pdf(506.95 KB) Additional Information: [full citation](#), [references](#), [citations](#)


2 [A sigma-delta modulation based BIST scheme for mixed-signal circuits](#)



Jiun-Lang Huang, Kwang-Ting Cheng

 January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Publisher: ACM Press

 Full text available: pdf(117.31 KB) Additional Information: [full citation](#), [references](#), [citations](#)


3 [A BIST scheme for on-chip ADC and DAC testing](#)



Jiun-Lang Huang, Chee-Kian Ong, Kwang-Ting Cheng

 January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: ACM Press

Full text available: pdf(114.67 KB)

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4 [A new algorithm for the design of stable higher order single loop sigma delta analog-to-digital converters](#)



S. R. Kadivar, D. Schmitt-Landsiedel, H. Klar

 December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society

Full text available: pdf(341.91 KB)

[Publisher Site](#)
 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)


Abstract: This paper presents a new algorithm to attain optimized network scaling in single loop, 1 bit Sigma Delta Analog 1d Digital Converters (SD ADC) of order three or more. The algorithm is based on a novel mathematical description of stability and performance criteria of the SD ADC and on the application of nonlinear interactive

optimization techniques. The feasibility of the new algorithm has been confirmed in practical implementations. The method brings new insight on the correlation bet ...

Keywords: CAD, SD ADC, analogue-digital conversion, convertors, electronic engineering computing, higher order, network scaling, nonlinear interactive optimization, performance criteria, sigma delta analog-to-digital converters, single loop

5 Theory of PLL fractional-N frequency synthesizers

A. Marques, M. Steyaert, W. Sansen

January 1998 **Wireless Networks**, Volume 4 Issue 1

Publisher: Kluwer Academic Publishers

Full text available:  [pdf\(482.69 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper presents an overview of the evolution of frequency synthesizers based on phase-locked loops (PLLs). The main limitations of the digital PLLs are described, and the consequent necessity of using fractional-N techniques is justified. The origin of the typical spurious noise lines on the sidelobes of the synthesized frequency is explained. It is shown how to eliminate these spurious noise lines by using digital \Delta\Sigma modulators to control the frequency division value. Finally ...

6 Wireless telecom silicon integration: analog design for radio, baseband and speech spectrum

J. Sevenhans, D. Haspeslagh, J. Wenin

January 1998 **Wireless Networks**, Volume 4 Issue 1

Publisher: Kluwer Academic Publishers

Full text available:  [pdf\(324.74 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)



The application today, pushing analog design for CMOS and RF-bipolar into new frontiers is definitely the mobile radio telephony. New telecom systems like GSM, PCN, DECT, DCS, Wireless in the loop...are all developing very rapidly and will enable us very soon to organise a complete telephone network with full coverage for your car, as well as in your kitchen and on your office desk. In Europe the major telecom companies have worked together to establish one common standard for cellular mobi ...

7 A Methodology for Designing Continuous-Time Sigma-Delta Modulators

Philippe Benabes, Mansour Keramat, Richard Kielbasa

March 1997 **Proceedings of the 1997 European conference on Design and Test**

Publisher: IEEE Computer Society

Full text available:  [pdf\(534.46 KB\)](#) Additional Information: [full citation](#), [abstract](#)
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A methodology for analysis and synthesis of lowpass sigma-delta (/spl Sigma//spl Delta/) converters is presented in this paper. This method permits to synthesize /spl Sigma//spl Delta/ modulators employing continuous-time filters from discrete-time topologies. The analysis method is based on the discretization of continuous-time model and using a discrete simulator which is more efficient than an analog simulator. Finally, a realistic design of a second-order /spl Sigma//spl Delta/ modulator wit ...

Keywords: sigma-delta modulation, design methodology, continuous-time sigma-delta modulator, continuous-time filter, discrete-time topology, discrete simulation, low-pass second-order /spl Sigma//spl Delta/ modulator, compensation, DAC


8 Detection of defective sensor elements using $\Sigma\Delta$ -modulation and a matched filter

D. Weiler, O. Machul, D. Hammerschmidt, B. J. Hosticka

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: ACM Press

Full text available:  pdf(88.57 KB) ; Additional Information: [full citation](#), [references](#), [index terms](#)

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9 Low power signal processing architectures for network microsensors

 Michael J. Dong, K. Geoffrey Yung, William J. Kaiser

August 1997 **Proceedings of the 1997 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available:  pdf(613.09 KB) Additional Information: [full citation](#), [references](#), [citations](#)

10 Metrics, techniques and recent developments in mixed-signal testing

Gordon W. Roberts

January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society

Full text available:  pdf(240.28 KB)

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Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper presents a tutorial on mixed-signal testing. Our focus is on testing the analog portion of the mixed-signal device, as the digital portion is handled in the usual way. We begin by first outlining the role of test in a manufacturing environment, and its impact on product cost and quality. We look at the impact of manufacturing defects on the behavior of digital and analog circuits. Subsequently, we argue that analog circuits require very different test methods than those presently used ...

Keywords: manufacturing defects, manufacturing environment, measurement setups, mixed analogue-digital integrated circuits, mixed-signal testing, product cost, quality

11 Proceedings of the SIGNUM conference on the programming environment for development of numerical software

 March 1979 **ACM SIGNUM Newsletter**, Volume 14 Issue 1

Publisher: ACM Press


Full text available:  pdf(5.02 MB) Additional Information: [full citation](#)

12 Pseudo-random testing and signature analysis for mixed-signal circuits

Chen-Yang Pan, Kwang-Ting Cheng

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society

Full text available:  pdf(88.30 KB)

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Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In this paper, we address the problem of functional testing of mixed-signal circuits using pseudo-random patterns. By embedding the linear, time-invariant (LTI) analog circuit between a digital-to-analog converter (DAC) and an analog-to-digital converter (ADC), we can model the analog and converter circuitry as a digital LTI system and test it using the pseudo-random vectors. We give mathematical analysis and formulate the pseudo-random testing process as the linear transformation of a random pr ...

Keywords: Pseudo-Random Testing, Random Process, Signature Analysis, Impulse Response

13 Approaches to On-chip Testing of Mixed Signal Macros in ASICs

R. A. Cobley

March 1996 **Proceedings of the 1996 European conference on Design and Test****Publisher:** IEEE Computer SocietyFull text available:  pdf(525.99 KB)Additional Information: [full citation](#), [abstract](#)[Publisher Site](#)

This paper initially researches the use of available low-cost analogue CMOS macros to perform simple on-chip tests on the Analogue to Digital Converter macro. The results are evaluated for these tests and then further fuller tests are undertaken. The technique of transient response testing is then applied to three CMOS analogue and mixed submacros to provide more comprehensive test results.

Keywords: Mixed signal ASICs, On-chip testing

14 Mixed-signal modelling in VHDL for system-on-chip applications

F. Pichon, S. Blanc, B. Candaele


March 1995 **Proceedings of the 1995 European conference on Design and Test****Publisher:** IEEE Computer SocietyFull text available:  pdf(486.17 KB)Additional Information: [full citation](#), [abstract](#), [citations](#)[Publisher Site](#)

Function transfer based modelling techniques are applied to the IEEE VHDL language to develop behavioral analogue models. This allows mixed-signal simulations integrated into a top-down ASIC design flow for system designers. An application to a clock module for a DSP-core ASIC, integrating a Phase-Locked Loop, demonstrates the usefulness of such an approach for the validation of large systems containing a small portion of analogue functionalities.


Keywords: DSP-core ASIC, VHDL, analogue functionalities, behavioral analogue models, circuit analysis computing, function transfer based modelling, hardware description languages, integrated circuit modelling, mixed analogue-digital integrated circuits, mixed-signal modelling, phase locked loops, phase-locked loop, system-on-chip applications, top-down ASIC design flow

15 Verifying Security

Maureen Harris Cheheyl, Morrie Gasser, George A. Huff, Jonathan K. Millen

September 1981 **ACM Computing Surveys (CSUR)**, Volume 13 Issue 3**Publisher:** ACM PressFull text available:  pdf(4.68 MB)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)16 Synthesis tools for mixed-signal ICs: progress on frontend and backend strategies

L. Richard Carley, Georges G. E. Gielen, Rob A. Rutenbar, Willy M. C. Sansen

June 1996 **Proceedings of the 33rd annual conference on Design automation****Publisher:** ACM PressFull text available:  pdf(91.08 KB)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)17 The HiBall Tracker: high-performance wide-area tracking for virtual and augmented environments

Greg Welch, Gary Bishop, Leandra Vicci, Stephen Brumback, Kurtis Keller, D'nardo Colucci

December 1999 **Proceedings of the ACM symposium on Virtual reality software and technology****Publisher:** ACM Press

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Our HiBall Tracking System generates over 2000 head-pose estimates per second with less than one millisecond of latency, and less than 0.5 millimeters and 0.02 degrees of position and orientation noise, everywhere in a 4.5 by 8.5 meter room. The system is remarkably responsive and robust, enabling VR applications and experiments that previously would have been difficult or even impossible. Previously we published descriptions of only the Kalman filter-based software approach that ...

Keywords: Kalman filter, autocalibration, calibration, delay, latency, optical sensor, sensor fusion, tracking, virtual environments

18 [A prototype framework for knowledge-based analog circuit synthesis](#)



R. Harjani, R. A. Rutenbar, L. R. Carley

June 1988 **Papers on Twenty-five years of electronic design automation****Publisher:** ACM PressFull text available:  pdf(1.06 MB)Additional Information: [full citation](#), [references](#), [index terms](#)

19 [Macromodeling of analog circuits for hierarchical circuit design](#)

Jianfeng Shao, Ramesh Harjani

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design****Publisher:** IEEE Computer Society PressFull text available:  pdf(933.09 KB)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Hierarchy plays a significant role in the design of digital and analog circuits. At each level of the hierarchy it becomes essential to evaluate if a sub-block design is feasible and if so which design style is the best candidate for the particular problem. This paper proposes a general methodology for evaluating the feasibility and the performance of sub-blocks at all levels of the hierarchy. A modified simplicial approximation technique is used to generate the feasibility macromodel and a ...

20 [A prototype framework for knowledge-based analog circuit synthesis](#)



R. Harjani, R. A. Rutenbar, L. R. Carley

October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation****Publisher:** ACM PressFull text available:  pdf(1.07 MB)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

An organization for a knowledge-based analog circuit synthesis tool is described. Analog circuit topologies are represented as a hierarchy of functional blocks; a planning mechanism is introduced to translate performance specifications between levels in this circuit hierarchy. A prototype implementation, OASYS, synthesizes sized transistor schematics for simple CMOS operational amplifiers from performance specifications and process parameters, and demonstrates the workability of the approach ...

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number of concurrent tasks or jobs, viewing their output on his display device as he desires. To achieve this goal the Virtual Terminal Management System (VTMS) converts a single physical terminal into multiple virtual terminals

24 Color portability—reality in the '90s (panel session)



Efraim Arazi, John D. Meyer, James A. Kasson

August 1990 **ACM SIGGRAPH 90 Panel Proceedings**

Publisher: ACM Press

Full text available: pdf(13.11 MB) Additional Information: [full citation](#), [index terms](#)



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1 [Analog design and evaluation: Jitter spectral extraction for multi-gigahertz signal](#)

Chee-Kian Ong, Dongwoo Hong, Kwang-Ting (Tim) Cheng, Li-C Wang

 January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**

Publisher: IEEE Press , IEEE Press

Full text available: pdf(512.61 KB)


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In this paper, we propose a method for extracting the spectral information of a multi-gigahertz jittery signal. This method may utilize existing on-chip single-shot period measurement techniques to measure the multi-gigahertz signal periods for spectral analysis. This method does not require an external sampling clock, nor any additional measurement beyond existing techniques. Experimental results show that this analysis method can accurately estimate the amount and frequencies of periodic and r ...

2 [Random Jitter Extraction Technique in a Multi-Gigahertz Signal](#)

Chee-Kian Ong, Dongwoo Hong, Kwang-Ting (Tim) Cheng, Li-C Wang

 February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 1**

Publisher: IEEE Computer Society

Full text available: pdf(227.01 KB)

 Additional Information: [full citation](#), [abstract](#), [index terms](#)

In this paper, we propose a simple technique for estimating the standard deviation of a Gaussian random jitter component in a multi-gigahertz signal. This method may utilize existing on-chip single-shot period measurement techniques to measure the multi-gigahertz signal periods for the estimation. This method does not require an external sampling clock, nor any additional measurement beyond existing techniques. Experimental results show that this extraction method can accurately estimate the ran ...

3 [Frontmatter \(TOC, Letters, Election results, Software Reliability Resources!, Computing Curricula 2004 and the Software Engineering Volume SE2004, Software Reuse Research, ICSE 2005 Forward\)](#)

 July 2005 **ACM SIGSOFT Software Engineering Notes**, Volume 30 Issue 4

Publisher: ACM Press

Full text available: pdf(6.19 MB)

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4

[An experiment in a user-oriented computer system](#)



Melvin Klerer, Jack May

May 1964 **Communications of the ACM**, Volume 7 Issue 5

Publisher: ACM Press

Full text available: [pdf\(617.47 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

A version of a software-hardware system for the purpose of facilitating the programming and analysis of well-formulated problems is described. A modified Flexowriter is used to generate computer-acceptable input when equations or computable requests are typed in much the same manner as they would appear in conventional mathematical texts. The typing and language rules are quite flexible and unrestrictive. While the compiler part is efficient, the system as a whole has much broader aspects a ...

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First Name = DERK

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|--------------------------|-------------------------|--------|------------|--|---------------|
| 09216255 | 6108401 | 150 | 12/18/1998 | METHOD OF STANDARD-LESS PHASE ANALYSIS BY MEANS OF A DIFFRACTOGRAM | REEFMAN, DERK |
| 09592059 | 6370490 | 150 | 06/12/2000 | METHOD OF DETERMINING AN INTRINSIC SPECTRUM FROM A MEASURED SPECTRUM | REEFMAN, DERK |
| 09855579 | 6690812 | 150 | 05/15/2001 | WATERMARK INSERTION AND EXTRACTION INTO AND FROM A HIGH QUALITY SIGNAL IS PERFORMED USING SAMPLE RATE CONVERSION | REEFMAN, DERK |
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First Name = ALPHONS

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
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